

Atty. Docket No. OPP-GZ-2007-0022-US  
Serial No: 10/736,063

Amendments to the Specification

Please replace the paragraph beginning at page 3, line 14, with the following replacement paragraph:

[0015] Subsequently, referring to FIG. 1c, using the polycrystalline silicon layer 15 as an etch-back, sidewall gates 15' are formed by leaving predetermined amounts of the polycrystalline silicon layer 15 on vertical wall areas of the nitride layer pattern 13'. In the etch-back forming process, a degree of over-etch is dictated by a desired gate width. That is, the smaller the desired gate width, the greater the amount of over-etch that needs to be performed such that the sidewall gates 15' are formed to a minimal width. As will be readily appreciated by those having ordinary skill in the art, it is possible to use an anisotropic etching process rather than an etch-back process[.].